

**LISTING OF THE CLAIMS:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1 (Currently Amended) A metal oxide semiconductor (MOS) device comprising:  
a semi-conducting substrate having source and drain regions;

a gate dielectric of less than 100 Å thickness on said semi-conducting substrate, said gate dielectric is selected from the group consisting of SiO<sub>2</sub>, nitrided SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, silicates or nitrogen additions of HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub> or La<sub>2</sub>O<sub>3</sub>, and mixtures thereof; and  
a gate formed of a metal comprising Re on top of said gate dielectric.

Claim 2 (Currently Amended) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric ~~layer having~~ has a thickness of less than 50 Å.

Claim 3 (Cancelled)

Claim 4 (Currently Amended) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric is ~~formed of a material~~ selected from the group consisting of Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, and mixtures thereof including silicates and nitrogen additions.

Claim 5 (Currently Amended) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is ~~formed of~~ SiO<sub>2</sub>.

Claim 6 (Cancelled)

Claim 7 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

Claim 8 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 9 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

Claim 10 (Currently Amended) A field effect transistor (FET) comprising:  
a semi-conducting substrate having at least one source and one drain region;  
a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate,  
said gate dielectric layer is selected from the group consisting of SiO<sub>2</sub>, nitrided SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, silicates or nitrogen additions of HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub> or La<sub>2</sub>O<sub>3</sub>, and mixtures thereof; and

a gate formed of a metal comprising Re on top of said gate dielectric layer.

Claim 11 (Currently Amended) A field effect transistor according to claim 10, wherein said gate dielectric layer ~~having~~ has a thickness of less than 50 Å.

Claim 12 (Cancelled)

Claim 13 (Currently Amended) A field effect transistor according to claim 10, wherein said gate dielectric layer is ~~formed of a material~~ selected from the group consisting of Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, ZrO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, and mixtures thereof including silicates and nitrogen additions.

Claim 14 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

Claim 15 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 16 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon.